

**AMENDMENTS TO THE SPECIFICATION:**

*Please amend the paragraph starting on line 5 of page 2 and ending on line 19 of page 2, as follows:*

A number of problems have been identified in the fields of reticle technology, photolithography and array-based ASICs. One such problem is the need for high volume production of master device templates that can be customized into several low volume products using customer specific reticles. Another problem is the need for Low Volume, customer specific, Reticles (LVRs) which consist of multiple device layers on a single reticle to be used concurrently in production with High Volume Reticles (HVRs) which consist of multiple instances of a single device layer on a reticle. Still another problem is the need for a pattern of the LVRs to register to the HVRs when printed on the wafer. Conversely, another problem is the need for a ~~patter~~ pattern of the HVRs to register to the LVRs when printed on the wafer. Yet another problem is the decrease in die per wafer due to wrapping a scribe around each die for both LVRs and HVRs for registration and end of line testing. Still another problem is the high cost of standard HVR sets relative to an LVR set custom order. Another problem is the prototype turnaround time of wafer processing associated with full LVR sets.

*Please amend the paragraph starting on line 7 of page 10 and ending on line 10 of page 11, as follows:*

The invention focuses on the process for Array-Based ASIC manufacturing in which both high volume production and small custom orders are relevant. Array-Based ASIC's offer the fastest customized implementation of a customer's logic onto a piece of silicon because of the

small number of reticles required to define the function of the chip. Diffusion layers are completed in large scale production. HVR reticles are best used for this process, as described hereinabove. These wafers then sit in inventory waiting for the personalization provided by the customer. Most Gate Array Product/Rapid Chip families will have several "masterslice" sizes available to allow for some reasonable selection of die size that comes closest to the size needed to implement customer logic. The front end of the diffusion "template wafers" will always contain more gates than will be used to implement the custom design simply because they have been built as general purpose pre-constructed pieces of silicon, specifically so that turn around time can be fast, since only the top few layers of metal must be processed to complete a design definition. This concept is ideal for designs that will either have relatively low production volume or for designs that may need ~~to be redone~~ to be redone because of design changes or enhancements. Since the custom orders will generally be small, the LVR reticle method lends itself well to the back end "custom" processing. Thus, for optimal production of Gate Array, Embedded Array, and Rapid Chip ~~products~~ a products, a method was needed in which LVR and HVR reticles could be used concurrently in the same set to build custom products. Large scale production of standard diffusion layers can be done with HVR reticles in which multiple instances of the device are exposed at a time. Then, for the configurable customer specific layers, LVR reticles are used to customize the back end of the devices.

*Please amend the paragraph starting at line 17 of page 11 and ending at line 3 of page 12, as follows:*

A standard LVR reticle 62 is illustrated in FIG. 4. The LVR reticle 62 is formed by first laying down an array of die 64, which is formed of multiple layers of different dies 64a, 64b, 64c, 64d. The array of die 64 is formed in a square pattern, in the illustrated embodiment the square pattern is 2x2. ~~Provided 2x2.~~ Provided below each dies 64a, 64b, 64c, 64d, is an X scribe 66 which are wrapped around the dies 64a, 64b, 64c, 64d. ~~Provided to the right of each die 64a, 64b, 64c, 64d, is a Y scribe 68 which are wrapped around the dies 64a, 64b, 64c, 64d.~~

*Please amend the paragraph starting at line 12 of page 13 and ending at line 11 of page 14, as follows:*

A method 140 of the invention is provided, and is illustrated in FIG. 10. The method 140 is a method of preparing a wafer 141 using the modified HVR reticle 120 and the LVR reticle 62. The method 140 begins with the step 142 of providing a standard LVR reticle 62, similar to that as illustrated in FIG. 4. The method 140 further begins with the step 144 of providing the modified HVR reticle 120, as illustrated in FIG. 8. The method 140 includes the step 146 of exposing the modified HVR reticle 120 onto the wafer 141. The method 140 includes the step 148 of blading out one of the dies 64a, 64b, 64c, 64d of the standard LVR reticle 62, for illustration purposes die 64a is bladed out. The method 140 further includes the step 150 of aligning the X scribe 66 of the bladed out die 64a with one of the X scribes 126a, 126b, 126c, 126d of the modified HVR reticle 120, for illustration purposes X scribe 66 is aligned with X scribe 126d. The method 140 further includes the step 152 of aligning the Y

scribe 68 of the bladed out die 64a with one of the Y scribes 128a, 128b, 128c, 128d of the modified HVR reticle 120, for illustration purposes Y scribe 68 is aligned with Y scribe 128d. The method 140 further includes the step 154 of exposing the bladed out die 64a on one of the dies 124 of the modified HVR reticle 120. In similar fashion, the bladed out die 64a can be exposed on the other dies 124 of the modified HVR reticle 120 as desired. Also in similar fashion, the other dies 64b, 64c, 64d of the standard LVR reticle 62 can be bladed out and exposed on the dies 124 of the modified HVR reticle 120 as desired.

*Please amend the paragraph starting at line 12 of page 14 and ending at line 19 of page 14, as follows:*

The method 140 provides for high volume production of base layers with HVR reticles which can then be set to inventory. From those base layer wafers, only a small number of LVR reticles need to be created to create a customer specific product. From a customer perspective, prototype turnaround time is thus decreased with respect to traditional methods. Designs that require a complete mask set (cell-based) will always require more time to manufacture than designs which ~~us~~ use a basic set of diffusion masks and only require customization at the metal layers (Array-Based).

*Please amend the paragraph starting at line 16 of page 15 and ending at line 8 of page 16, as follows:*

A method 200 is thus described and illustrated in FIG. 11, to overcome this problem. The method 200 is aimed at reducing the scribe width in order to pack die more efficiently on the

wafer. In a traditional scribe there are structures used for registration and structures used for electrical testing of the finished product. Registration marks are needed around each die for LVR to HVR alignment, however, the scribeline transistors related to wafer testing are not necessary around every die. There are multiple types of transistors in the scribe and their physical properties are defined in the diffusion (HVR) layers of processing. Even though the functionality of these structures are different, the metal back end layers (processed with LVR reticles) are identical for these transistors. The method 200 is directed at scribes ~~have~~ having P and N type transistors therein. It should be noted, however, that the method 200 applies to any scribeline structures of which functionality is defined in HVR masking layers and share common patterns on LVR masking layers.